

**In The Claims:**

**Claims 1-4 (canceled)**

Claim 5 (original) A chip structure with test pads thereon, at least comprising:  
a chip with an active surface having at least a flip-chip bonding pad and at  
least a test pad thereon, wherein the test pad is positioned on the peripheral section  
of the active surface and is electrically connected to the flip-chip bonding pad; and  
a passivation layer formed over the active surface, wherein the passivation  
layer exposes the flip-chip bonding pad.

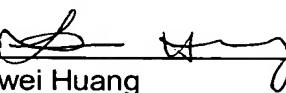
Claim 6 (original) The chip structure of claim 5, wherein the chip furthermore  
comprises at least a fuse line buried within the chip and a fuse window having an  
upper surface below the active surface of the chip for decreasing the thickness of  
the structure above the fuse line such that the passivation layer fills the fuse window.

Claim 7 (original) The chip structure of claim 5, wherein the chip furthermore  
comprises at least a trace line on the active surface for connecting the test pad to  
the flip-chip bonding pad and the passivation layer also covers the trace line.

Claim 8 (original) The chip structure of claim 5, wherein the chip furthermore  
comprises a bump attached to the flip-chip bonding pad.

Respectfully submitted,

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